

Improve PCB gold-plating yields using DOE

Full-body electrolytic gold plating during PCB manufacture has been a troublesome process. It has been associated with the production of excessive amounts of gold-plating scrap caused by photoresist breakdown. To overcome this problem a circuit board company, which builds boards containing 4 to 40 layers each—roughly 1,500 layers each day, applies Design of Experiments (DOE) techniques to its gold-plating line.

The gold-plating process in PCB manufacturing has been plagued by excessive loss of gold-plating scrap caused by photoresist breakdown. DOE will help you identify the responsible factors and offer solutions to overcome the problem.

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and two-factor interactions are measurable. Also the fewest number of boards are sacrificed while producing statistically accurate results.

tributor to the breakdowns (figure 1). In the case of Factor B, plating production operators had been trying to ensure void-free holes by flashplating panels at the beginning of the line.

After flash-plating, operators would then begin to scrub the panels with Scotch-bright and pumice before photoresist lamination (factor B's high level as shown in Table 1). This particular cleaning method, however, did not leave a consistently uniform surface.

Factor	Low level	High level
Resist type	Product A	Product B
Post-flash clean	Flash/Electroless	Flash/Pumice/Re-flash
Laminator roll temperature	105°C	125°C
Exposure level	Step 22	Step 26
Solder strip method	2 Tanks	Conveyor

Table 1: Consider five factors for the DOE, which you think, are responsible for the production of gold-plating scrap.

Choosing factors and levels

The experimenters chose five factors and five levels to study (Table 1), then input their choices into a DOE software package (Design-Ease software). These were factors affecting the photoresist imaging process prior to gold plating. The DOE package screened the factors and possible interactions, which contributed to resist breakdown.

Due to the high cost of rework usually encountered in a gold plating process, the experimenters limited their tests to five factors in 16 experiments. Several other advantages justify this decision. Apart from being reliable and fast, all the main effects

Analyzing the results

The design experiment results analyzed by the DOE software exhibited extreme variations. While some test panels showed no resist breakdowns, others manifested up to 600 defects.

Further study with the software revealed that the interaction of Factor B (post-flash cleaning method) and Factor E (solder strip method) was a statistically significant con-

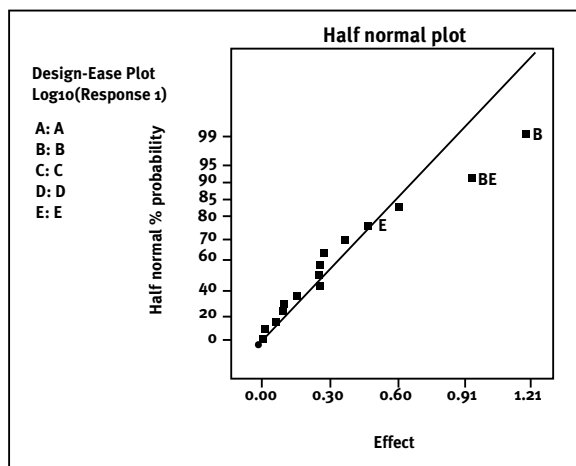


Figure 1: You can easily identify significant interaction between post-flash (B) and solder-strip (E) cleaning. Also note the significance of factor B alone. Factors on or about the line indicate normality.

What is Design of Experiments (DOE)?

DOE provides information about how factors such as time, temperature, or photoresist type interact in a system. It simultaneously evaluates multiple factors within a process, offering a tool for circuit board fabrication.

DOE is superior to traditional one-factor-at-a-time (OFAT) ex-

perimentation because OFAT needs a number of runs to obtain equivalent knowledge of a process. Moreover, OFAT cannot reveal the results of interactions between different system parameters.

Although DOE was invented in the 1920s, it re-

mained unused because it required laborious hand calculations. Today, off-the-shelf, statistically sound DOE software can be easily set up and used.

High-end DOE software costing less than US\$1,000 now fits data into mathematical equations and predicts outcomes for any combination of values. You can further optimize these responses and identify combinations that best serve your needs. **ee**

Two methods were used to solder-strip PCBs (Factor E). One was a two-component two-tank system—the low level (Table 1). The other method utilized was a conveyor solder strip method—the high level.

The continuous interactions between post-flash cleaning and solder strip (**figure 2**) have clearly indicated that the highest yields are attained by running the line at low-level B and high-level E. The gold-plating process was therefore modified to run only a flash/electroless process, while the tank solder strip process was eventually eliminated.

A second DOE run

The second DOE specifically addressed the electrolytic nickel-gold process. Again, five factors were studied (**Table 2**).

Upon carefully analyzing the results gathered with the DOE software, the experimenters learned that two of the factors—318 acid cleaner and HCL-predip—significantly contributed to resist breakdown during gold plating.

Surprisingly, the resist breakdown was lower when the 318 acid cleaner was used at the higher level (at higher temperature and for longer dwell time). This usually happens because the photoresist eventually hardens during the process, thereby reducing resist breakdown caused by nickel plating chemistry.

The presence of chlorides in the HCL-predip eventually weakens the photore-

sist, thus allowing gold to leach under the resist. Based on these DOE findings, HCl has now been replaced with a sulfuric predip.

You can thus improve yield through process optimization, and significantly reduce rework by incorporating DOE in your production line. DOE offers real-world solutions to your gold plating yield issues, with production settings and procedures that are repeatable and statistically valid.

Armed with understandable and detailed graphs and images produced by the DOE software package, you can identify and solve problems that hinder production line efficiency. **ee**

Factor	Low level	High level
318 Acid-T&T	32°C, 1 min.	46°C 6 min.
Microetch	10µm	50µm
Ni-asf/thick	1A	3A
HCL-predip	30 sec.	5 min.
Gold strike	No	Yes

Table 2: The DOE software identified 318 acid cleaner and HCL-predip as major contributors to resist breakdown during the electrolytic Ni-Au process.

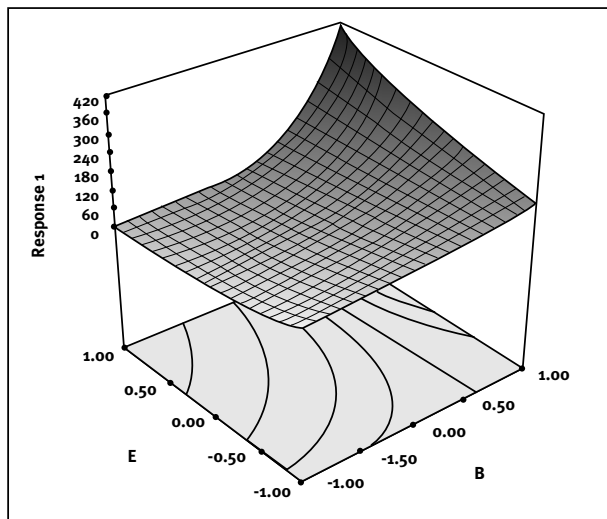


Figure 2: Factor B run at a low level and Factor E run at its high level minimizes defects. This means that you should clean the boards first by flashplating, then electroless. Use the conveyor method during solder-strip.

You may send your comments on this article to Mark Anderson through e-mail at info@statease.com, or fax: 1-612-3782152.